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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/633,673	08/05/2003	Ilia Ovsiannikov	M4065.0734/P734	6886

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EXAMINER	
GILES, NICHOLAS G	

ART UNIT	PAPER NUMBER
2622	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/633,673	OVSIANNIKOV ET AL.	
	Examiner	Art Unit	
	Nicholas G. Giles	2622	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 October 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,5,18-51 and 56-86* is/are pending in the application.

4a) Of the above claim(s) *18-51 and 56-66* is/are withdrawn from consideration.

5)☒ Claim(s) *75-79 and 84-86* is/are allowed.

6)☒ Claim(s) *1-3,5,67-74 and 80-83* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 August 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 10/09/2007 has been entered.

Response to Arguments

2. Applicant's arguments filed 10/09/2007 have been fully considered but they are not persuasive.

Regarding claim **67**, applicant argues that a "reset transistor having a source/drain regions on opposite sides of a gate of the reset transistor, one of the source/drain regions being switchably coupled to a first and second voltage and the other of the source/drain regions being coupled to a node and the gate of the reset transistor being coupled to a reset control circuit" is not shown. The examiner points out that in Fig. 4B of Kole the reset transistor S1 has reset input 72 that in 8:4-9 it can be seen that the reset input changes between high and low values. In order to accomplish this there must be some circuit means controlling the reset input 72. Further it can be seen in Fig. 4B that reset transistor S1 has one of its source/drain terminals connected to select input 71 and the other to the node formed between reset transistor S1, image

sensor 20, and amplifier 30. Further in 8:4-9 Kole explains that the select input 71 can take a high or low value.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims **1-3, 5, 67-74, and 81-83** rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

5. Claim **1** recites the limitation "reset transistor control circuit". There is insufficient antecedent basis for this limitation in the claim. Examiner will treat this to be the "reset control circuit"

Claims **2, 3, 5, and 83** depend on claim 1 and therefore are rejected.

6. Claim **67** recites the limitation "a reset control circuit" at the end of the claim. There is insufficient antecedent basis for this limitation in the claim. The limitation was previous recited and the examiner will treat the repeated limitation at the end of the claim to read "said reset control circuit"

Claims **68-70** depend on claim 67 and therefore are rejected.

7. Claim **71** recites the limitation "controlled voltage source" in line 9. There is insufficient antecedent basis for this limitation in the claim. The examiner will treat this to read "controllable voltage source".

8. Claim **71** recites the limitation "second voltage level" in lines 14 and 18. There is insufficient antecedent basis for this limitation in the claim. The examiner will treat this to read "second higher voltage level".

Claims **72-74** depend on claim 71 and therefore are rejected.

9. Claim **73** recites the limitation "first voltage level". There is insufficient antecedent basis for this limitation in the claim. The examiner will treat this to read "first lower voltage level".

Claim **74** depends on claim 73 and therefore is rejected.

10. Claim **74** recites the limitation "pixel". There is insufficient antecedent basis for this limitation in the claim. The examiner will treat this to read "photosensor".

11. Claim **74** recites the limitation "said sample and hold". There is insufficient antecedent basis for this limitation in the claim. The examiner will treat this to read "said sample and hold circuit".

12. Claim **81** recites the limitation "storage node" in lines 3 and 6. There is insufficient antecedent basis for this limitation in the claim. The examiner will treat this to read "charge storage region".

13. Claim **81** recites the limitation "first supply voltage". There is insufficient antecedent basis for this limitation in the claim. The examiner will treat this to read "first reset supply voltage".

Claim **82** depends on claim 81 and therefore is rejected.

14. Claim **82** recites the limitation "storage region". There is insufficient antecedent basis for this limitation in the claim. The examiner will treat this to read "charge storage region".

Note that the examiner has cited all of the antecedent errors found, however more may be present.

Claim Objections

15. Claim **81** is objected to because of the following informalities: Line 4 repeats the limitation "said first reset supply voltage at". This should be "said first reset supply voltage and". Appropriate correction is required.

16. Claim **81** objected to because of the following informalities: Line 5 has the words "is" and "are" next to each other. The word "are" should be deleted. Appropriate correction is required.

Claim Rejections - 35 USC § 102

17. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

18. Claims **80-81** are rejected under 35 U.S.C. 102(e) as being anticipated by Kole (U.S. Patent No. 6,501,064).

Regarding claim **80**, Kole discloses:

> A pixel comprising: a first voltage source having an output switchable between a first and second reset supply voltage in response to a first control signal (select input 71 can take a high or low value 7:15-8:10); a charge storage region (between reset transistor S1, image sensor 20, and amplifier 30 in Fig. 4B); a reset transistor connected between said first voltage source and said charge storage region (reset transistor S1); and a control circuit for providing a gate control voltage to a gate of said reset transistor, said control circuit selectively providing a first operating control voltage (high) and a second operating control voltage (low) to said reset transistor, said second operating control voltage being less than said first operating control voltage (there must be some circuit means controlling the reset input 72 in order to control reset input to go from low to high).

Regarding claim **81**, see the rejection of claim 80 and note that Kole further discloses:

> First voltage source and said control circuit are configured to operate said reset transistor such that a first reset voltage is provided at said charge storage region when said first reset supply voltage and said second operating control voltage is provided to said reset transistor (8:1-

10, sensor 20 (Fig. 4B) is in selected state after integration, select input 71 is high, and reset input 72 is low), and a second reset voltage is provided at said charge storage region when said first reset supply voltage and said first operating control voltage are provided to said reset transistor (sensor 20 is reset, select input 71 is high, reset input 72 is high).

Claim Rejections - 35 USC § 103

19. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

20. Claims **67, 68, and 70** are rejected under 35 U.S.C. 103(a) as being unpatentable over Kole (U.S. Patent No. 6,501,064) in view of Merrill (U.S. Pub. No. 2002-0036700).

Regarding claim **67**, Kole discloses:

An imaging device, comprising: a processor (inherent); an imager array coupled to said processor, one pixel of said image array comprising: a charge sharing node (between reset transistor S1, image sensor 20, and amplifier 30); and a reset transistor having source/drain regions on opposite sides of a gate, one of said source/drain regions being switchably coupled to a first and second voltage (reset transistor S1 has reset input 72 that in 8:4-9 it can be seen that the reset input changes between high

and low values or voltages as shown in 7:37-43), the other of said source/drain regions being coupled to said node (7:15-8:10).

Kole is silent with regards to a row select transistor being switchably connected to the first and second voltages and the reset transistor and row select transistor having their own separate control lines/circuits. Merrill discloses this in ¶0043-0045 and Fig. 7. Note that the row select transistor is after the amplifier and thus would be switchably connected to the high and low levels of select input 71. An advantage to using a row transistor is that rows of pixels can be selectively read out. An advantage to having separate control lines/circuits for the reset transistor and row select transistor is that pixels can be selectively reset and rows can be selectively read out. For this reason it would have been obvious to one of ordinary skill in the art at the time the invention was made to have Kole include a row select transistor being switchably connected to the first and second voltages and the reset transistor and row select transistor having their own separate control lines/circuits.

Regarding claim **68**, see the rejection of claim 67 and note that Kole further discloses:

First voltage is higher than said second voltage (7:15-8:10).

Regarding claim **70**, see the rejection of claim 67 and note that Kole further discloses:

One of said source/drain regions is coupled to only one of said first and second voltages at a time (7:15-8:10).

21. Claim **69** is rejected under 35 U.S.C. 103(a) as being unpatentable over Kole (U.S. Patent No. 6,501,064) in view of Kokubun et al. (U.S. Pub. No. 2003/0146993) in further view of Merrill (U.S. Pub. No. 2002-0036700).

Regarding claim **69**, see the rejection of claim 68 and note that Kole discloses a low signal level during integration as a second voltage. Kole is silent with regards to the second voltage being ground potential. Kokubun et al. discloses this in ¶0055 and Fig. 4 where M22 can be seen connected to ground, which is a low signal level. An advantage to doing so is that ground potential is further away from a transistor "turn on" voltage than an arbitrary low signal level voltage thus avoiding a partial transistor "turn on". For this reason it would have been obvious to one of ordinary skill in the art at the time the invention was made to have Kole's low signal level be ground potential.

Allowable Subject Matter

22. Claims **75-79 and 84-86** are allowed.

Regarding claim **75**, no prior act could be located that teaches or fairly suggests the claimed structure in combination with the claimed operating limitations (control signals and voltages) during the claimed time intervals (first, second, third).

Regarding claims **76-79**, these claims depend on claim 75 and therefore are allowed.

Regarding claim **84**, no prior art could be located that teaches or fairly suggests the claimed sampling limitations during the claimed sample and hold period in combination with the claimed reset transistor receiving the claimed signals.

Regarding claims **85-86**, these claims depend on claim 84 and therefore are allowed.

23. Claims **1-3, 5, 83, and 71-74** would be allowable if rewritten or amended to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action.

Regarding claim **1**, no prior art could be located that teaches or fairly suggests the claimed structure in combination with the claimed operating limitations (control signals and voltages) during the claimed time intervals (first, second, third).

Regarding claims **2, 3, 5, and 83**, these claims depend on claim 1 and therefore would be allowable if claim 1 was allowed.

Regarding claim **71**, no prior art could be located that teaches or fairly suggests the claimed operating condition limitations during the first and second time periods for the claimed structure.

Regarding claims **72-74**, these claims depend on claim 71 and therefore would be allowable if claim 71 was allowed.

24. Claim **82** would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

Regarding claim **82**, no prior art could be located that teaches or fairly suggests the third voltage, second reset supply voltage, and first operating control voltage in the

claimed structure and operating signals and voltages in combination with the rest of the limitations of the claim.

25. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nicholas G. Giles whose telephone number is (571) 272-2824. The examiner can normally be reached on Monday through Friday from 7:30am to 4:00pm EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lin Ye can be reached on (571) 272-7372. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

NGG

LIN YE
SUPERVISORY PATENT EXAMINER